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AP99-002B

November 17, 2003

To: Commissioner for Patents
Office of Initial Patent Examination
Customer Service Center
P.O. Box 1450
Alexandria, VA 22313-1450

From: Stephen B. Ackerman

Subject: Serial No.: 10/616,751
Filing Date: 07/10/03
Inventor: P. W. Lee, et al
Title: Stacked Gate Flash Memory Cell with Reduced Disturb
Conditions

REQUEST TO CORRECT FILING RECEIPT

Dear Sir:

On the copy of the enclosed Filing Receipt, there is an error in the Title. The word "Disturb" is misspelled in the Title. The corrected Title reads: **Stacked gate flash memory cell with reduced disturb conditions.**

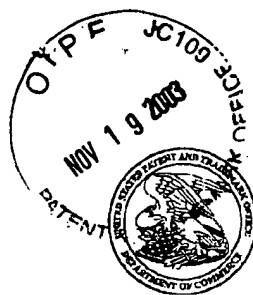
Please make the necessary change to correct the error on the Filing Receipt.

If there are any questions, please contact the undersigned attorney at (845) 452-5863. Thank you for your attention to this matter.

Respectfully Submitted,


Stephen B. Ackerman, Reg. No. 37,761

OCT. 12 2003



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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/616,751	07/10/2003	2818	375	AP99-002B	4	6	1

CONFIRMATION NO. 2335

George O. Saile
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FILING RECEIPT



OC000000011008027

Date Mailed: 10/08/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Peter W. Lee, Saratoga, CA;
Hsing-Ya Tsao, Santa Clara, CA;
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Assignment For Published Patent Application

APLUS FLASH TECHNOLOGY, INC.;

Domestic Priority data as claimed by applicant

This application is a DIV of 09/531,787 03/21/2000

Foreign Applications**If Required, Foreign Filing License Granted:** 10/08/2003**Projected Publication Date:** 01/15/2004**Non-Publication Request:** No**Early Publication Request:** No**** SMALL ENTITY ****

Title

Stacked gate flash memory cell with reduced distrib conditions

Preliminary Class

365

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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